copy of US patent number 6,104,068 is provided herewith for the Examiner's convenience. The Examiner's attention is directed in particular to Figure 2 and the accompanying description therewith of US patent number 6,104,068. Applicant respectfully request that reference to this illustrative patent be addressed in the Examiner's next response.

IN THE SPECIFICATION

The specification was objected as being misdescriptive. The objection states that:

> Page 10, lines 16-30, describes the pair of transistors M3, M5 and M4, M6 of each inverter, B1 and B2, comprises a dual-gated MOSFET. It is well known in the art that a dual-gated transistor is an AND function circuit. However, the pair of transistors M3, M5 and M4, M6 are the OR function circuit. Therefore, the pair of transistors M3, M5 and M4, M6 can not be replaced with a dual-gated transistor.

The Examiner's restatement of the previous objection to the specification appears to entirely ignore the Applicant's response thereto and, in particular, refuses to address the fact that there is more that one type of dual-gate transistor. That is, in the art there are dual gated transistor having two gates only on one side of a transistor, e.g. Cuevas, and there are dual gated transistors having each gate on opposite sides of the transistor. Applicant has invited the Examiner to confirm the same in reference to US patent number 6,104,068 which further supports the Applicant's lexicography. Applicant respectfully renew its request that reference to this illustrative patent be addressed as evidencing that dual gated transistors have been described, by the present inventor, which perform the OR function. All dual-gated transistors do not perform the AND function. Certainly the one shown in Cuevas does, but this is not the entire universe of dual gate transistor types. Applicant's reference to US patent number 6,104,068 evidences this very fact.